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Keynote title: Toward Energy-Efficient HPC Systems with Dynamic Power-Performance Adjustment

Bio

Yasutaka Wada is a professor at the School of Information Science at Meisei University, Tokyo, Japan. Before joining Meisei University in 2015, he was an assistant professor at Waseda University, Tokyo, Japan, an assistant professor at the University of Electro-Communications, Tokyo, Japan, a junior researcher at Waseda University, and a research associate at the same university. He was also an associate professor at Egypt-Japan University of Science and Technology (E-JUST), Alexandria, Egypt, from 2010 to 2012.

He received his Ph.D. in computer science and engineering from Waseda University in 2009. His research and development activities cover various computer systems, from embedded systems to high-performance computing environments, to realize high-performance, energy-efficient, and easy-to-use computer systems. He is a member of ACM, IEEE Computer Society, IEICE, and IPSJ.

Toward Energy-Efficient HPC Systems with Dynamic Power Performance Adjustment

Abstract:

HPC systems' performance has been improved by increasing amounts of resources such as the number of processor cores, accelerator devices, memory sizes, and interconnection bandwidth. However, we are now facing power and energy problems even with HPC systems due to the limitation of power supply and cooling capabilities. Unlike embedded systems, though we can continue increasing the hardware resources for our future HPC systems, HPC systems are required to maximize their performance under the given power budget.

This means that power and energy supply are substantial restrictions to improve their performance, and it is necessary to overcome this problem with software techniques that are cooperative with hardware functionalities. In this talk, I would like to introduce our research effort and activities to realize energy-efficient HPC systems with application optimization methods for dynamic power-performance adjustment on HPC applications, including DVFS and approximate computing techniques. Power-performance modeling for each application will be the key to applying them dynamically in a more fine-grained manner at runtime.

Accuracy-performance modeling will also be essential for approximate computing methods to optimize the tradeoff among performance, power/energy, and accuracy of the results. Understanding hardware and application characteristics would be necessary to obtain accurate and efficient power-performance and accuracy-performance models for each application.